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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U. S. PATENT: 7029971 CASE NO.: EL0513USNA

PATENTEE: BORLAND ET AL. ART UNIT: 2818

ISSUED: APRIL 18, 2006 CONFIRMATION NO.: 1472

EXAMINER: DUNG ANH LE

ASSIGNED: E. I. DU PONT DE NEMOURS AND COMPANY

FOR: THIN FILM DIELECTRICS FOR CAPACITORS AND METHODS OF MAKING THEREOF

REQUEST FOR EXPEDITED CERTIFICATE OF CORRECTION

Via EFS-Web

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to MPEP 1480.1, the patentees through their attorney hereby respectfully request the expedited correction of the printing error shown on the attached Form PTO/SB/44 through the expedited issuance of a Certificate of Correction in this patent.

Remarks, which begin on page 2, present good and sufficient reasons for the expedited issuance and for patentee's lack of financial responsibility for the Certificate of Correction fee under 37 C.F.R. 1.20(a).

REMARKS

Status of the Patent

[1] U.S. Pat. No. 7,029,971 ["the patent"] issued 16 April 2006 and is still in force from Application No. 10/621,796 filed 17 July 2003 ["the application"]. The patent issued with an incorrect dependency for granted claim 16. Claim 16 should depend from claim 15; instead, the patent reads that claim 16 depends from claim 1.

Prosecution History of the Patent

[2] There were 30 claims as filed. A copy of the originally filed claims as they appear on PAIR is attached in Appendix 1. The original claims are marked to show that: original claim 19 depended from claim 18. As discussed below, claim 19 became granted claim 16, which depended from granted claim 15. As filed, the claims recited the correct dependency.

[3] The application published 20 Jan 2005. A copy of the published claims as it appears on PAIR is attached in Appendix 2. The published claims are marked to show that: original claim 19 depended from claim 18. As discussed below, claim 19 became granted claim 16, which depended from granted claim 15. As published, the claims recited the correct dependency.

[4] In response to the only Office Action, Applicants responded on 28 April 2005. A copy of this response as it appears on PAIR is attached in Appendix 3. The amended claims as marked show that: claim 19 was NOT amended to depend from claim 1. Instead, claim 19 depended from claim 18. As discussed below, claim 19 became granted claim 16, which depended from granted claim 15. The amended claims recited the correct dependency.

Occurrence of the Printing Error

[5] In the response to the sole Office Action, claims 2 and 3 were canceled and claim 10 was rewritten in independent format. The claims were thereafter allowed. There were 28 allowed claims.

[6] In printing the allowed claims, the PTO renumbered original claim 10 to become claim 28 and then renumbered the remaining claims accordingly. Original claim 19 became granted claim 16. The attached evidence shows that claim 19, which after renumbering became granted claim 16, never changed its dependency on claim 18, which became granted claim 15.

[7] The dependency of claim 16 changed only during the printing of the patent and thus, the error in claim 16 was made solely by the PTO.

Justification for Expedited Issuance of a Certificate of Correction

[8] MPEP §1480.1 requires patentees to demonstrate that the printing error is an error of consequence and was made solely by the Patent and Trademark Office.

[9] The discussion in ¶¶3-8 above demonstrates that the error was made solely by the PTO. Patentees respectfully request that the submission fee for the attached Form be waived pursuant to MPEP§1480.

[10] The error is of consequence because the error affects the validity of claim 16. Claim 16 as printed depends from claim 1 and is in effect a duplicate of claim 7. Claim 16 should properly depend from claim 15, which means that ultimately claim 16 defines a variation of the method of claim 12. As it now reads, claim 16 does not recite a separate variation of the method of claim 12 but rather a variation of claim 1 that duplicates the embodiment recited in Claim 7. In effect, the error has caused patentees not to be granted the full boundaries of the property that the PTO allowed during the examination.

[11] Since the printing error was made solely by the PTO and is of consequence, patentees respectfully assert that the conditions for expedited issuance of Certificate of Correction pursuant to MPEP §1480.1 have been met.

[12] Patentees' representative respectfully requests that she be contacted by telephone should other information be needed to satisfy this request for expedited issuance of a Certification of Correction.

[13] Attachments:

a. Appendix 1: Original Claims as Filed
b. Appendix 2: Claims as Published
c. Appendix 3: Claims as Amended during Prosecution
d. Form PTO/SB/44

Respectfully submitted,

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Dated: 10 Jan 2008

Appendix 1

CLAIMS

What is claimed is:

1. A method of making a capacitor, comprising:

providing a bare metallic foil;

forming a dielectric over the bare metallic foil, wherein forming the dielectric comprises:

forming a dielectric layer over the foil;

annealing the dielectric layer;

re-oxygenating the dielectric resulting from the annealing; and

forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form the capacitor.

2. The method of Claim 1, wherein annealing comprises:

annealing at a temperature in the range of about 800-1050°C.

3. The method of Claim 2, wherein annealing comprises:

annealing in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres.

4. The method of Claim 2, wherein annealing results in a dielectric comprising crystalline barium titanate or crystalline barium strontium titanate.

5. The method of Claim 1, wherein forming a dielectric layer comprises:

providing a dielectric precursor solution comprising barium acetate and at least one of titanium isopropoxide and titanium butoxide.

6. The method of Claim 1, wherein the capacitor has a capacitance density of at least 0.5 microFarad/cm^2.

7. The method of Claim 1, wherein re-oxygenating the dielectric comprises:

re-oxygenating the dielectric at a temperature in the range of 450-700°C and an oxygen partial pressure in the range of 10^{-2} to 10^{-7} atmospheres.

8. The method of Claim 1, wherein providing a bare metallic foil comprises:

providing a bare copper foil.

9. The method of Claim 1, wherein providing a bare metallic foil comprises:

providing a foil that has not been treated with organic additives.

10. The method of Claim 1, wherein the dielectric layer is applied to a first side of the foil, the method comprising:

forming a second dielectric layer on a second side of the foil opposite to the first side.

11. The method of Claim 1, wherein forming a dielectric comprises:

forming a dielectric having a thickness in the range of about 0.2-2.0 microns.

12. The method of Claim 1, wherein forming a dielectric comprises:

forming a doped dielectric.

13. The method of Claim 1, comprising:

etching the conductive layer.

14. A capacitor formed by the method of Claim 1.

15. A method of making a capacitor, comprising:

providing a metallic foil;

forming a dielectric over the metallic foil, wherein forming a dielectric comprises:

annealing at a temperature of greater than about 800°C in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres;

re-oxygenating the dielectric; and

forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form the capacitor.

16. The method of Claim 15, wherein annealing comprises:

annealing at a temperature in the range of about 800-1050°C.

17. The method of Claim 15, wherein annealing results in a dielectric comprising barium titanate or barium strontium titanate.

18. The method of Claim 15, wherein providing a metallic foil comprises:

providing a bare copper foil.

19. The method of Claim 18, wherein providing a bare copper foil comprises:

providing a copper foil that has not been treated with organic additives.

20. The method of Claim 15, wherein forming a dielectric comprises:

forming a dielectric having a thickness in the range of about 0.2-2.0 microns.

21. The method of Claim 15, comprising:

etching the conductive layer.

22. A capacitor formed by the method of Claim 15.

23. A method of making a capacitor, comprising:

providing a bare copper foil that has not been treated with organic additives;

forming a dielectric having a thickness in the range of about 0.2-2.0 microns over the copper foil, wherein forming a dielectric comprises:

annealing at a temperature in the range of about 800-1050°C in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres, wherein the dielectric comprises at least one of barium titanate and barium strontium titanate;

re-oxygenating the dielectric at a temperature in the range of about 450-700°C; and

forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form a capacitor.

24. A capacitor formed by the method of Claim 23.

25. A method of making a printed wiring board, comprising:

forming one or more capacitors using any of the methods recited in claims 1, 15 or 23;

laminating the one or more capacitors with one or more laminate layers; and

forming connection circuitry, wherein the connection circuitry connects to one or more conductive layers or foils of the one more capacitors.

26. The method of Claim 25, wherein forming connection circuitry comprises:

forming one or more conductive vias.

27. The method of Claim 25, comprising:

connecting one or more conductive layers to a voltage pin of an integrated circuit by way of the connection circuitry.

28. The method of Claim 25, comprising:

etching one or more conductive layers before forming connection circuitry.

29. The method of Claim 28, wherein etching forms two separate electrodes from a conductive layer.

30. A printed wiring board formed by the method of Claim 25.

Appendix 2

surface of the dielectric **212**. The entire upper surface of the dielectric **212** may be covered by the layer **220**. The electrode layer **220** may be plated with copper to a desired thickness at this stage or at a later stage. **18** microns is a suitable thickness in one embodiment. A laminate dielectric material **230** is laminated to the dielectric **214**, and a conductive foil **240** is laminated to the laminate dielectric material **230**.

[**0101**] The conductive layer **220** and the foil **240** may be imaged and etched to form any desired combination of electrodes and interconnect circuitry. Vias may also be formed in the article shown in **FIG. 17**. **FIG. 18** illustrates the article of **FIG. 17** after etching, and after incorporation into the printed wiring board **2000**.

[**0102**] The printed wiring board **2000** may be formed in a manner similar to the printed wiring board **1000** illustrated in **FIGS. 14 and 15**. The innerlayer panel in the printed wiring board **2000** comprises a bottom electrode **202** formed from the foil **200**, a dielectric **216**, a dielectric **218**, top electrodes **222, 224**, and circuitry **242**. The electrode **202**, the dielectric **216** and the electrodes **222, 224** form a capacitor structure **205**. In the capacitor structure **205**, the electrode **202** serves as a common electrode to the electrodes **222, 224**, which correspond to capacitors **226, 228**, respectively. The printed wiring board **2000** may be similar to the printed wiring board **1000**, and like elements in **FIG. 18** are labeled with like reference numbers to those of the printed wiring board **1000**, preceded by a "2" instead of a "1."

[**0103**] The capacitor structure **205** has dielectrics **216, 218** disposed on either side of the foil electrode **202**. Cladding the electrode **202** in dielectrics **216, 218** creates a balanced structure that equalizes strain on both sides of the foil used as the substrate (foil **200** in **FIG. 16**). Therefore, strain during cooling from annealing temperatures is minimal, and the foil **200** therefore is less likely to be warped during cooling.

[**0104**] The printed wiring boards **1000, 2000** may correspond to many different component types. For example, the printed wiring boards **1000, 2000** may be mother-boards, integrated circuit packages or packaging substrates, integrated passive devices, or interposer devices. Embedded capacitors in the printed wiring boards **1000, 2000** may be connected to, for example, integrated circuits, and may be used for functions such as decoupling, energy storage or other functions requiring high capacitance. The electrodes of the capacitors in the printed wiring boards **1000, 2000** can be connected to terminals, such as voltage pins, of integrated circuits by connection circuitry.

[**0105**] The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only selected preferred embodiments of the invention, but it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings, and/or within the skill or knowledge of the relevant art.

[**0106**] The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments, not explicitly defined in the detailed description.

What is claimed is:

1. A method of making a capacitor, comprising:

providing a bare metallic foil;

forming a dielectric over the bare metallic foil, wherein forming the dielectric comprises:

forming a dielectric layer over the foil;

annealing the dielectric layer;

re-oxygenating the dielectric resulting from the annealing; and

forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form the capacitor.

2. The method of claim 1, wherein annealing comprises:

annealing at a temperature in the range of about 800-1050° C.

3. The method of claim 2, wherein annealing comprises:

annealing in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres.

4. The method of claim 2, wherein annealing results in a dielectric comprising crystalline barium titanate or crystalline barium strontium titanate.

5. The method of claim 1, wherein forming a dielectric layer comprises:

providing a dielectric precursor solution comprising barium acetate and at least one of titanium isopropoxide and titanium butoxide.

6. The method of claim 1, wherein the capacitor has a capacitance density of at least 0.5 microFarad/cm^2.

7. The method of claim 1, wherein re-oxygenating the dielectric comprises:

re-oxygenating the dielectric at a temperature in the range of 450-700° C. and an oxygen partial pressure in the range of 10^{-2} to 10^{-7} atmospheres.

8. The method of claim 1, wherein providing a bare metallic foil comprises:

providing a bare copper foil.

9. The method of claim 1, wherein providing a bare metallic foil comprises:

providing a foil that has not been treated with organic additives.

10. The method of claim 1, wherein the dielectric layer is applied to a first side of the foil, the method comprising:

forming a second dielectric layer on a second side of the foil opposite to the first side.

11. The method of claim 1, wherein forming a dielectric comprises:

forming a dielectric having a thickness in the range of about 0.2-2.0 microns.

Appendix 3

AMENDED CLAIMS

1. (Amended herein) A method of making a capacitor, comprising:
providing a bare metallic foil;
forming a dielectric over the bare metallic foil, wherein forming the dielectric comprises:
forming a dielectric layer over the foil;
annealing the dielectric layer; wherein annealing comprises:
annealing at a temperature in the range of about 800-1050°C and annealing comprises annealing in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres;
re-oxygenating the dielectric resulting from the annealing; and
forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form the capacitor.

2. Cancelled

3. Cancelled

4. (Amended herein) The method of Claim ~~3~~ 1, wherein annealing results in a dielectric comprising crystalline barium titanate or crystalline barium strontium titanate.

5. (Original) The method of Claim 1, wherein forming a dielectric layer comprises:
providing a dielectric precursor solution comprising barium acetate and at least one of titanium isopropoxide and titanium butoxide.

6. (Original) The method of Claim 1, wherein the capacitor has a capacitance density of at least 0.5 microFarad/cm^2.

7. (Original) The method of Claim 1, wherein re-oxygenating the dielectric comprises:
re-oxygenating the dielectric at a temperature in the range of 450-700°C and an oxygen partial pressure in the range of 10^{-2} to 10^{-7} atmospheres.

8. (Original) The method of Claim 1, wherein providing a bare metallic foil comprises:
providing a bare copper foil.

9. (Original) The method of Claim 1, wherein providing a bare metallic foil comprises:

providing a foil that has not been treated with organic additives.

10. (Amended herein) ~~The method of Claim 1,~~ A method of making a capacitor, comprising:

providing a bare metallic foil;

forming a dielectric over the bare metallic foil, wherein forming the dielectric comprises:

forming a dielectric layer over the foil;

annealing the dielectric layer;

re-oxygenating the dielectric resulting from the annealing; and

forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form the capacitor

wherein the dielectric layer is applied to a first side of the foil, the method comprising:

forming a second dielectric layer on a second side of the foil opposite to the first side.

11. (Original) The method of Claim 1, wherein forming a dielectric comprises:
forming a dielectric having a thickness in the range of about 0.2-2.0 microns.

12. (Original) The method of Claim 1, wherein forming a dielectric comprises:
forming a doped dielectric.

13. (Original) The method of Claim 1, comprising:
etching the conductive layer.

14. (Original) A capacitor formed by the method of Claim 1.

15. (Original) A method of making a capacitor, comprising:
providing a metallic foil;
forming a dielectric over the metallic foil, wherein forming a dielectric comprises:
annealing at a temperature of greater than about 800°C in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres;
re-oxygenating the dielectric; and
forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form the capacitor.

16. (Original) The method of Claim 15, wherein annealing comprises:
annealing at a temperature in the range of about 800-1050°C.

17. (Original) The method of Claim 15, wherein annealing results in a dielectric comprising barium titanate or barium strontium titanate.

18. (Original) The method of Claim 15, wherein providing a metallic foil comprises:
providing a bare copper foil.

19. (Original) The method of Claim 18, wherein providing a bare copper foil comprises:
providing a copper foil that has not been treated with organic additives.

20. (Original) The method of Claim 15, wherein forming a dielectric comprises:
forming a dielectric having a thickness in the range of about 0.2-2.0 microns.

21. (Original) The method of Claim 15, comprising:
etching the conductive layer.

22. (Original) A capacitor formed by the method of Claim 15.

23. (Original) A method of making a capacitor, comprising:
providing a bare copper foil that has not been treated with organic additives;
forming a dielectric having a thickness in the range of about 0.2-2.0 microns over the copper foil, wherein forming a dielectric comprises:
annealing at a temperature in the range of about 800-1050°C in an environment having an oxygen partial pressure of less than about 10^{-8} atmospheres, wherein the dielectric comprises at least one of barium titanate and barium strontium titanate;
re-oxygenating the dielectric at a temperature in the range of about 450-700°C; and
forming a conductive layer over the dielectric, wherein the metallic foil, the dielectric, and the conductive layer form a capacitor.

24. (Original) A capacitor formed by the method of Claim 23.

25. (Original) A method of making a printed wiring board, comprising:
forming one or more capacitors using any of the methods recited in claims 1, 15 or 23;

laminating the one or more capacitors with one or more laminate layers; and

forming connection circuitry, wherein the connection circuitry connects to one or more conductive layers or foils of the one more capacitors.

26. (Original) The method of Claim 25, wherein forming connection circuitry comprises:

forming one or more conductive vias.

27. (Original) The method of Claim 25, comprising:

connecting one or more conductive layers to a voltage pin of an integrated circuit by way of the connection circuitry.

28. (Original) The method of Claim 25, comprising:

etching one or more conductive layers before forming connection circuitry.

29. (Original) The method of Claim 28, wherein etching forms two separate electrodes from a conductive layer.

30. (Original) A printed wiring board formed by the method of Claim 25.